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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,637	09/28/2000	Gary Dan Dotson	00AB152	8211

7590 06/02/2003

Allen-Bradley Company, Inc.
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EXAMINER	
HAVAN, THU THAO	
ART UNIT	**PAPER NUMBER**
2672	5

DATE MAILED: 06/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,637	DOTSON ET AL.	
	Examiner	Art Unit	
	Thu-Thao Havan	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Claims 1-**33** are pending in the present application.

Response to Arguments

2. Applicant's arguments filed March 18, 2003 have been fully considered but they are not persuasive. As addressed below, Potter et al. and Aranda teach the claimed limitations.

A.) In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., an improved raster engine with a multiple color depth digital display interface) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

B.) Potter teaches a raster engine for interlacing a frame buffer in a computer system to one of a plurality of disparate displays (col.3, lines 3-51; figs. 1 and 3) when he discloses display device such as element 170 of figure 1. Specifically, column 3, lines 3-6 discloses a display device. Claim is only referring to one display device since it claims "a frame buffer in a computer system to one of a plurality of disparate displays."

C.) Potter discloses at least one control register programmable via the computer system to select a display mode (col. 5, line 60 to col. 6, line 3; fig. 1—element 125 is a type of

control register). In figure 1 of Potter, there are numerous control devices to select a display mode. Element 157, 160, and 125 are all control register.

D.) Potter discloses a logic device having a parallel output (col. 7, lines 50-67). In other words, the parallel gradient producing unit corresponds to a parallel output since a producing unit is a type of output.

E.) Aranda teaches a dual port RAM device (col. 1, line 15 to col. 2, line 33; abstract). In other words, Aranda discloses dual interleave DRAMs for improved bandwidth. Furthermore, he teaches dividing the entire frame buffer into two separate devices so that the characteristics of adjacent pixels can be alternately stored in different ones of the two devices.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-**33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Potter et al. (US patent no. 6,157,393) in view of Aranda (US patent no. 5,321,809).

Re claim 1, Potter teaches a raster engine for interlacing a frame buffer in a computer system to one of a plurality of disparate displays (col.3, lines 3-51), comprising at least one control register programmable via the computer system to select a display mode (col. 5, line 60 to col. 6, line 3; fig. 1—element 125 is a type of

control register); and a logic device having a parallel output (col. 7, lines 50-67), the logic device being adapted to select appropriate pixel data from the dual port RAM device according to the selected display mode (col. 8, line to col. 10, line 23; col. 14, lines 28-64; fig. 3a), to remap the selected pixel data according to the selected display mode, and to provide remapped selected pixel data at the parallel output according to a universal routing scheme applicable to the plurality of disparate displays (col. 10, line 7 to col. 13, line 65). In other words, Potter teaches each graphics processor includes first and second graphical data ports that each interface with the graphical data either transmitted to or received from other graphics processors. In that the graphics processor that processes graphical data for display on a display device includes a state input that receives state data identifying the number of other graphics processors being utilized with the graphics processor, a pixel processor that produces a second amount of graphical data during each clock cycle of a reference clock, and first and second graphical data ports that each interface with graphical data either transmitted to or received from other graphics processors when in a multiple state.

However, Potter fails to explicitly teach a dual port RAM device. But Potter teaches a master RAM and a slave RAM that are equivalence to a dual port RAM device (col. 8, line 10, line 23; col. 14, lines 28-64; fig. 3a—elements 242a and 242b are two types of RAM). On the other hand, Aranda specifically teaches a dual port RAM device for interfacing a frame buffer in a computer system. Therefore, taking the combined teaching of Potter and Aranda as a whole, it would have been obvious to combine the teaching of Aranda to the system of Potter because doing so would have

enabled dividing the entire frame buffer into two separate devices so that the characteristics of adjacent pixels can be alternately stored in different ones of the two devices as noted in Aranda (col. 1, line 15 to col. 2, line 33).

Re claims **21, 26, and 30**, Potter teaches a raster engine for interlacing a frame buffer in a computer system to one of a plurality of disparate displays (col.3, lines 3-51), comprising at least one control register programmable via the computer system to indicate a selected display mode (col. 5, line 60 to col. 6, line 3; fig. 1—element 125 is a type of control register); means for programming the at least one control register (col. 5, line 60 to col. 6, line 3); means for selecting appropriate pixel data from the frame buffer according to the selected display mode (col. 7, lines 50-67), and means for providing the selected pixel data to an output device according to the selected display mode (col. 8, line to col. 10, line 23; col. 14, lines 28-64; fig. 3a).

Re claims **2, 5-6, 12-17, 23, 27-28, and 31-32**, Potter discloses the selected display mode comprises one of single pixel per clock up to 24 bits wide, single 16 bit 565 pixel per clock... (col. 3, line 65 to col. 4, line 53; col. 10, lines 7-50; col. 11, line 18 to col. 13, line 65). Potter teaches multiple types of bits wide for the interface system in relation to frame buffer.

Re claims **3, 7, 9-11, 24-25, 29, and 33**, Aranda discloses one of a look up table, a grayscale generator, and a blink logic system, wherein the logic device receives the selected pixel data from the dual port RAM device via the one of the look up table, the grayscale generator, and the blink logic system according to the selected display mode (col. 6, line 33 to col. 8, line 64; figs. 1-2 and 7).

Re claims 4, 8, 18-19, 22, Potter discloses a multiplexer (col. 3, line 35 to col. 5, line13; col. 5, line 60 to col. 7, line 49). A multiplexer is a device for funneling several different streams of data over a common communications line. Thus, figures 1 and 2b illustrated the multiplexer.

Re claims 20, the limitation of claim 20 is identical to claim 1 above. Therefore, claim 20 is treated with respect to grounds as set forth for claim 1 above.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiries

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thu-Thao Havan whose telephone number is (703) 308-7062. The examiner can normally be reached on Monday to Thursday from 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (703) 305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Thu-Thao Havan
May 21, 2003

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600